SYSTEMS AND METHODS FOR SYNCHRONIZING A SIGNAL ACROSS MULTIPLE CLOCK DOMAINS

ABSTRACT

An integrated circuit configured to capture an input signal to produce an output signal. The input signal is synchronized with a first clock signal. The output signal is synchronized with a second clock signal having a second frequency different from a first frequency associated with the first signal. The integrated circuit includes a first clock domain gating circuit having a first output terminal and a first input terminal. The first clock domain gating circuit is configured to be clocked by the first clock. The first input terminal is coupled to receive the input signal, and the first clock domain gating circuit is configured to toggle a state of a signal on the first output terminal from one of a first state and a second state to the other of the first state and the second state every time a pulse is detected in the input signal, thereby producing a latched output at the first output terminal. The integrated circuit also includes a second clock domain gating circuit having a second output terminal and a second input terminal. The second clock domain circuit is clocked by the second clock. The second input terminal is coupled to the first output terminal to receive the latched output, and the second clock domain gating circuit is configured to produce a pulse on the output signal at the second output terminal, with the pulse on the output signal having a duration at least as long as a period of the second clock every time a state of the latched output changes.